REMARKS

The specification and claims 3 and 5 have been amended to add "larger" after "driveability" as noted in the Official Action to place the application in condition for allowance at the time of the next Official Action.

Claims 1-2 were rejected as anticipated by COOPERMAN et al. 5,329,185. Claims 1-2 have been canceled and withdrawal of the rejection is respectfully requested.

Claims 3-6 were rejected as unpatentable over KOJIMA 6,510,542 in view of COOPERMAN et al. Reconsideration and withdrawal of the rejection are respectfully requested.

Claim 3 defines a repeater in a signal transmission line in a semiconductor device, where the repeaters divide the signal transmission lines into divided signal lines. Each repeater has two logic gates, the first logic gate having a larger driveability than the second logic gate.

KOJIMA describes a repeater in a signal transmission line in a semiconductor device, and the Official Action acknowledges that the repeater does not have two logic gates where the first logic gate has a larger driveability than the second logic gate. This is similar to the admitted prior art that describes a repeater with two logic gates, where the first

logic gate has a smaller driveability than the second logic gate. The Official Action looks to COOPERMAN et al. for motivation to modify the repeater in KOJIMA so that the driveability of the two logic gates is opposite that of the admitted prior art.

COOPERMAN et al. describes a connection between two logic systems that have incompatible voltage requirements. In particular, the connection is between an ECL circuit that operates at a first voltage and a CMOS circuit that operates at a second voltage. The connection suggested by COOPERMAN et al. changes the voltage levels of the CMOS circuit so that the two logic systems can be operably connected. One of the problems with the connection is that the relatively small voltage differential of the ECL circuit degrades the speed of the CMOS circuit (column 1, lines 21-40). The solution to this problem is to increase the size of the CMOS transistors in a first inverter stage 21A to compensate for the low ECL input swing of 800 millivolts at the input to the CMOS circuit. In other words, COOPERMAN et al. suggests increasing the size of the first inverter stage to make up for an insufficient voltage swing.

Applicant does not believe that one of skill in the art would look to COOPERMAN et al. for motivation to modify the repeater in KOJIMA so that the driveability of the two logic gates is opposite that of the admitted prior art because COOPERMAN et al. suggests a solution to a voltage problem that

does not exist in the repeaters of the prior art (such as KOKIMA and the admitted prior art).

As explained in the background of the present application, when the capacitance of each of the divided signal lines is lower than an input capacitance of a respective one of the repeaters connected thereto, suitable repeaters have two logic gates, where the first logic gate has a smaller driveability than the second logic gate (i.e., M>1). However, the present inventor is the first to notice that in some signal transmission lines (e.g., long signal transmission lines; page 14, lines 9-19) the capacitance of the each of the divided signal lines is higher than an input capacitance of a respective one of the repeaters connected thereto and to suggest that the traditional approach with M>1 does not work well when this capacitance is higher.

Accordingly, the inventor proposes to reverse the conventional approach so that the driveability of the first logic gate is larger than that of the succeeding logic gate. This solution is particularly applicable where the capacitance of the each of the divided signal lines is higher than an input capacitance of a respective one of the repeaters connected thereto. In other words, the inventor has found that the selection of the driveability of the two logic gates is a function of distance.

Returning to the COOPERMAN et al., one of skill in the art (a) would recognize the acceptability of the admitted prior art in which the driveability of the two logic gates is opposite that claimed herein (recall that the prior art does not recognize the capacitance problem addressed for the first time by the present inventor), (b) would see that COOPERMAN et al. proposes a solution to a voltage problem that does not exist in the repeater of the prior art, (c) would not find sufficient motivation in COOPERMAN et al. to modify the admitted prior art that works in an acceptable manner, and (d) therefore would not make the suggested combination of references. That is, COOPERMAN et al. suggests a way to increase speed when a particular problem occurs that does not occur in the repeaters herein and thus the artisan would not ignore the admitted prior art and turn to this reference to modify KOJIMA.

Accordingly, claims 3-6 avoid the rejection under §103.

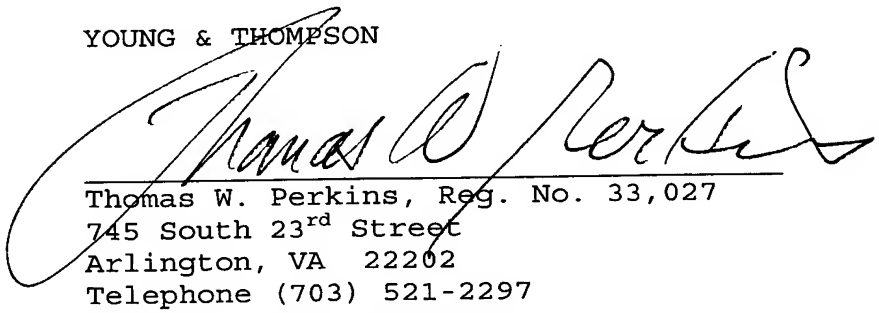
New claims 7-8 have been added that explicitly include the capacitance of the divided signal lines. There is no suggestion in the references to include this feature and thus the new claims are further distinguishable from the art of record.

In view of the present amendment and the foregoing remarks, it is believed that the present application has been placed in condition for allowance. Reconsideration and allowance are respectfully requested.

The Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 25-0120 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17.

Respectfully submitted,

YOUNG & THOMPSON



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